REMARKS

Entry of this Amendment is proper because it narrows the issues on appeal and does not require further searching by the Examiner.

Claims 2-8, 10-12, 14-20 and 22-24 are all the claims presently pending in the present Application. Claims 2-8, 20-12 and 14-16 have been amended to more particularly define the claimed invention. Claims 1, 9, 13 and 21 have been canceled.

While the claim amendments made herein may help to distinguish the invention over the prior art, Applicant's intention in making the amendments is for the purpose of particularly pointing out the invention, and not for the purpose of distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability. Further, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 2-12, 14-20 and 22-24 stand rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Mahalingam (U. S. 6,205,503) in view of Horst (U. S. 5,867,501).

This rejection is respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

An exemplary aspect of the claimed invention (e.g., as recited, for example, in **claim 2**) is directed to a computer system including a plurality of central processing unit (CPU) and memory installed apparatuses including a CPU and a memory, a plurality of input/output control apparatuses which are assigned to the plurality of CPU and memory installed apparatuses, respectively, and communicate with the plurality of CPU and memory installed apparatuses via a network, and a plurality of diagnostic control circuits which are connected to the plurality of the CPU and memory installed apparatuses and the plurality of input/output control apparatuses.

Importantly, a CPU and memory installed apparatus of the plurality of CPU and memory installed apparatuses includes communication means for transmitting an input/output instruction issued by a CPU of the CPU and memory installed apparatus to an input/output control apparatus assigned to the CPU and memory installed apparatus via the network,

and receives a response from the input/output control apparatus via the network, the input/output control apparatus includes communication means for receiving the input/output instruction from the CPU and memory installed apparatus assigned to the input/output control apparatus via the network, and transmits a response to the input/output instruction to the CPU and memory installed apparatus via the network, and the plurality of diagnostic control circuits includes a diagnostic control circuit connected to the CPU and memory installed apparatus and input/output control apparatus, and if the diagnostic control circuit detects a fault in the CPU and memory installed apparatus, then the diagnostic control circuit determines an other CPU and memory installed apparatus of the plurality of CPU and memory installed apparatuses which will use the an input/output control apparatus (Application at Figure 8; page 34, line 25-page 35, line 22).

These features may allow the claimed invention to increase the availability of the computer system if the computer system suffers a fault (Application at page 51, lines 19-20).

II. THE FINALITY OF THE OFFICE ACTION IS PREMATURE AND SHOULD BE WITHDRAWN

Applicant notes that MPEP 706.07(a) provides that "second or any subsequent actions on the merits shall be final, except where the examiner **introduces a new ground of rejection** that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement .." (emphasis added).

Applicant notes that the Office Action includes a new ground of rejection (e.g., claims 2-12, 14-20 and 22-24 now stand rejected under 35 USC 103(a) as allegedly unpatentable over Mahalingham (US 6,205,503) in view of Horst (US 5,867,501)). The Examiner states on page 10 of the Office Action that "Applicant's amendment necessitated the new ground(s) of rejection", but **independent claims 2, 14 and 16 were not even amended in the Amendment** filed on May 26, 2009. Instead, Applicant simply pointed out that the Examiner's rejection (e.g., claims 2-12, 14-20 and 22-24 were rejected under 35 USC 103(a) as allegedly unpatentable over Mahalingham (US 6,205,503) in view of Suzuki (US 6,854,081) was improper because Suzuki is **not 35 USC 103(a) prior art against the present Application**). Therefore, **the May 26th Amendment clearly did not "necessitate the new ground(s) of rejection"**, and the finality of the July 15, 2009 Office Action should

be withdrawn.

III. THE ALLEGED PRIOR ART REFERENCES

The Examiner alleges that Mahalingam would have been combined with Horst to form the invention of claims 2-12, 14-20 and 22-24.

In particular, Applicant submits that these alleged references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

In fact, Applicant submits that the alleged references provide no motivation or suggestion to urge the combination as alleged by the Examiner. Indeed, these alleged references clearly do not teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the alleged references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Mahalingam, nor Horst, nor any alleged combination thereof, teaches or suggests "*wherein a CPU and memory installed apparatus of said plurality of CPU and memory installed apparatuses comprises communication means for transmitting an input/output instruction issued by a CPU of the CPU and memory installed apparatus to an input/output control apparatus assigned to said CPU and memory installed apparatus via said network, and receives a response from said input/output control apparatus via said network, wherein said input/output control apparatus comprises communication means for receiving the input/output instruction from the CPU and memory installed apparatus assigned to said input/output control apparatus via said network, and transmits a response to said input/output instruction to said CPU and memory installed apparatus via said network, and wherein said plurality of diagnostic control circuits comprises a diagnostic control circuit connected to the CPU and memory installed apparatus and input/output control apparatus, and if said diagnostic control circuit detects a fault in the CPU and memory installed apparatus, then the diagnostic control circuit determines an other CPU and memory installed apparatus of the plurality of CPU and memory installed apparatuses which will use the an input/output control apparatus*", as recited, for example, in claim 2 (Application at Figure 8; page 34, line 25-page 35, line 22). As noted above, these features

may allow the claimed invention to increase the availability of the computer system if the computer system suffers a fault (Application at page 51, lines 19-20).

Clearly, these novel features are not taught or suggested by the cited references.

Indeed, Applicant would first point out that it is not clear in the Office Action what features in Mahalingam the Examiner is relying as allegedly teaching a plurality of CPU and memory installed apparatuses or a plurality of input/output control apparatuses. The Examiner on page 2 of the Office Action simply refers Applicant to Figures 2 and 3. Applicant notes that there are many features depicted in Figures 2 and 3 of Mahalingam, but none of the features are identified as a "CPU and memory installed apparatus" and none of the features are identified as an "input/output control apparatus".

Applicant notes that Figures 2 and 3 disclose plural CPUs 200 and a memory controller 204 connected to a bus, but nowhere in Figures 2 and 3 (or anywhere else) does Mahalingam teach or suggest a plurality of central processing unit (CPU) and memory installed apparatuses including a CPU and a memory, and a plurality of input/output control apparatuses which are assigned to the plurality of CPU and memory installed apparatuses, respectively, and communicate with the plurality of CPU and memory installed apparatuses via a network. In fact, Mahalingam describes Figure 2 as showing "a multiple bus configuration connecting I/O adapters and a network of microcontrollers" to clustered CPUs of a computer system, and describes Figure 3 as showing "a multiple bus configuration connecting canisters containing I/O adapters and a network of microcontrollers" to clustered CPUs of a computer system (Mahalingam at col. 6, lines 35-43).

Moreover, the Examiner alleges on page 3 of the Office Action that Mahalingam teaches a communication means of a CPU and memory controlled apparatus at Figure 2 and col. 4, lines 28-50. However, this passage simply teaches a secondary processor in addition to the usual processor for handling I/O transactions, and that the secondary processor is located on an input/output platform which controls a plurality of I/O devices. However, nowhere does this passage teach or suggest a "communication means" of a CPU and memory installed apparatus, as in the claimed invention.

The Examiner alleges on page 3 of the Office Action that Mahalingam teaches a communication means of an input/output control apparatus at Figure 2, col. 4, lines 28-50 and col. 5, line 65-col. 6, line 15. However, the passage at col. 5, line 65-col. 6, line 15 simply teaches a method of "hot swapping" an input/output platform. Nowhere in this passage or anywhere else

does Mahalingam teach or suggest a "communication means" of an input/output control apparatus, as in the claimed invention.

Further, nowhere does Mahalingam teach or suggest a plurality of diagnostic control circuits including a diagnostic control circuit connected to the CPU and memory installed apparatus and input/output control apparatus, and if the diagnostic control circuit detects a fault in the CPU and memory installed apparatus, then the diagnostic control circuit determines an other CPU and memory installed apparatus of the plurality of CPU and memory installed apparatuses which will use the an input/output control apparatus. Indeed, the Examiner expressly concedes on pages 3-4 of the Office Action that Mahalingam does not teach or suggest these features.

Likewise, Horst does not teach or suggest these features. However, Horst simply discloses a method of encoding data which is completely unrelated to the computer system of the claimed invention. Indeed, the Examiner attempts to rely on Figures 4 and 5, and col. 18, lines 35-50, and col. 82, lines 45-50 and col. 83, lines 20-50 to support his position. However, these passages simply teach interface units 24a, 24b "to respectively communicate processors 20a, 20b to the memory controllers" (Horst at col. 18, lines 35-36), that a router 14A reporting a bad link (TLB) to a CPU 12A (Horst at col. 82, lines 45-50), and a scenario in which CPU 12A sustains a fault and a the next I/O transmission, one of the routers 14A, 14B will detect a divergence (Horst at col. 83, lines 20-27).

That is, nowhere in these passages or anywhere else does Horst teach or suggest a CPU and memory installed apparatus of the plurality of CPU and memory installed apparatuses includes communication means for transmitting an input/output instruction issued by a CPU of the CPU and memory installed apparatus to an input/output control apparatus assigned to the CPU and memory installed apparatus via the network, and receives a response from the input/output control apparatus via the network, the input/output control apparatus includes communication means for receiving the input/output instruction from the CPU and memory installed apparatus assigned to the input/output control apparatus via the network, and transmits a response to the input/output instruction to the CPU and memory installed apparatus via the network, and the plurality of diagnostic control circuits includes a diagnostic control circuit connected to the CPU and memory installed apparatus and input/output control apparatus, and if the diagnostic control circuit detects a fault in the CPU and memory installed apparatus, then the diagnostic control circuit determines an other CPU and memory installed apparatus of the plurality of CPU and

memory installed apparatuses which will use the an input/output control apparatus, as in the invention of claim 2.

Therefore, Horst clearly does not make up for the deficiencies of Mahalingam.

Therefore, Applicant submits that these alleged references would not have been combined and even if combined, the alleged combination would not teach or suggest the features of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 2-8, 10-12, 14-20 and 22-24, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Date: 10/6/09

Respectfully submitted,

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Amendment Under 37 CFR §1.116 by facsimile with the United States Patent and Trademark Office to Examiner Thuong Nguyen, Group Art Unit 2455 at fax number (571) 273-8300 this 6th day of October, 2009.

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